# An Overview of Altera SoC Design Advantages

## User-Customizable SoC Advantages

There has been much publicity in the industry about the new breed of user-customizable SoC devices and what they can do to improve your system design process and system performance. While there are some obvious advantages to integrating the processor and surrounding logic which yields improved system performance and functionality at a much lower system cost, you might be wondering if using a programmable SoC makes sense compared to an ASIC SoC implementation. Since today's SoC FPGAs use 28nm process technology with a move in 2014 to 20nm technology, the performance is comparable to an ASIC SoC implementation but without the high design engineering cost and high chip NREs associated with the ASIC version.

One of the keys to getting good results in a programmable SoC implementation is to make sure you select the best device architecture, but it really does matter when you want the best results. A designer should look at their proposed SoC architecture in terms of each of these categories:

- System Performance
- Reliability
- Flexibility
- System Cost
- Power Consumption
- Future Roadmap
- Development Tools

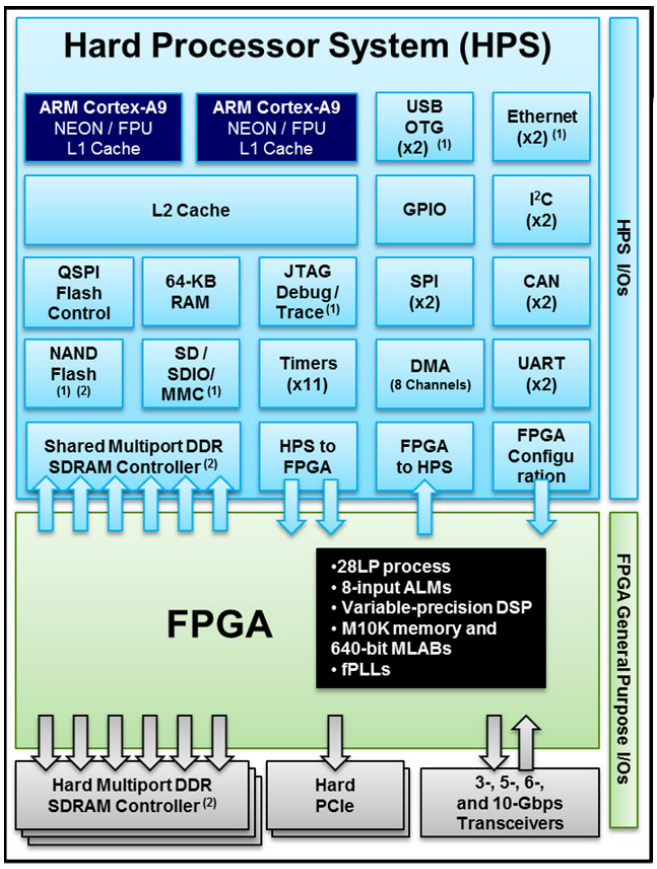
The Altera® SoC FPGAs such as the Cyclone® V SoC device used on the Mpression Helio *View* development platform has advantages in all of these areas, but the three that really stand out when you start to develop designs on them are the system performance and flexibility advantages and the way the development tools integrate the design tasks and make your design teams get a working design up and running faster and with less headache.

## Altera SoC Architecture Overview

Altera SoC devices integrate an ARM-based hard processor system (HPS) consisting of processor, peripherals, and memory interfaces, with FPGA fabric using a high-bandwidth interconnect backbone. It combines the performance and power savings of hard intellectual property (IP) with the flexibility of programmable logic.

These user-customizable ARM-based SoCs are ideal for:

- Reducing system power, cost, and board size by integrating discrete processors and digital signal processing (DSP) functions into a single FPGA
- Improving system performance via high-bandwidth interconnect between the processor and the FPGA
- Differentiating your end product by customizing in both hardware and software
- Enhancing system reliability with built-in error correction code (ECC) and memory protection guarding your system against potential hardware or software errors
- Developing ARM-compatible software with unmatched target visibility, control, and productivity using Altera's exclusive FPGA-adaptive debugging




**Notes:**
**(1) Integrated direct memory access (DMA)**
**(2) Integrated ECC**

These devices include additional hard logic such as PCI Express, multiport memory controllers, and high-speed serial transceivers. SoCs drive down power and cost while enabling performance levels required by cost-sensitive applications.

Flexibility and performance go hand-in-hand when using Altera SoCs. The designer has the flexibility to allocate functions to hardware or software freely within the chip, and even change the usage later without affecting the chip pin out or board layout. If the software team finds that their processors are being overload with tasks that are compute-intensive, you can easily decide to create custom hardware to accelerate those tasks and off load the processor.

This flexibility would not be useful if you don't have the performance in the CPU to FPGA interfaces. In the Altera SoCs, the HPS has multiple high-bandwidth interfaces between the HPS and FPGA logic with up to 125 Gbps of total throughput. In addition to the high bandwidth data capability, there is a second, low-latency, non-blocking, "lightweight" interconnect bridge optimized for control access that does not affect the usage of the 32, 64, or 128 bit wide data bridges.

The Altera SoC devices contain dedicated DDR SDRAM controllers for both the ARM HPS and the FPGA logic, both of them with integrated ECC error correction. In order to save cost in SoC FPGA applications, the FPGA logic can optionally access HPS memory through the processor's DDR memory controller. This could limit performance, but in the case of the Altera SoC devices, the 256 bits of data from the FPGA logic to the HPS DDR memory controller have direct connections without any intermediate switches or interconnect, allowing up to 9,600 MB per second peak memory bandwidth.

The Altera SoC FPGAs are unique in the industry in offering one to three hard DDR memory controllers, depending on device type, for the FPGA logic that are also capable of high speed memory access and can be used to off load memory access bandwidth from the processor memory controller in very performance sensitive applications.

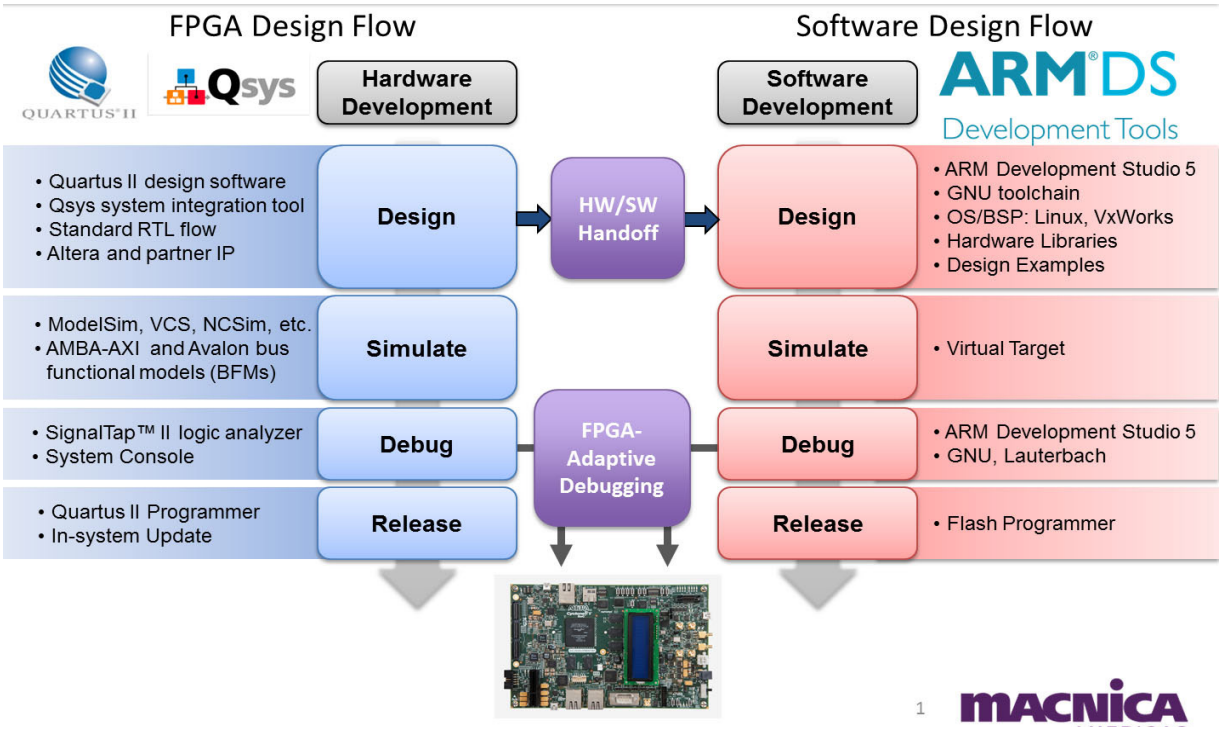
Both the processor and FPGA memory controllers implement ECC for not only the L1 cache in the processor, but also the L2 cache, external DDR memory access in both 16-bit and 32-bit modes, on-chip RAM and other data controllers such as the NAND controller, SD/MMC/SDIO controller, DMA controller, Ethernet controller, and USB controller.

## Altera SoC Design Tools

This performance and flexibility means that the design of the software and hardware are very interrelated since distribution of functions between the two domains will need to be handled by both design teams, since one designer rarely does all the hardware and software design for the system. In many cases, though, the hardware designer will want to run some simple test programs on the embedded processors to verify proper communication with the hardware he is designing and prove out other basic operations before getting the rest of the software team involved for application coding.

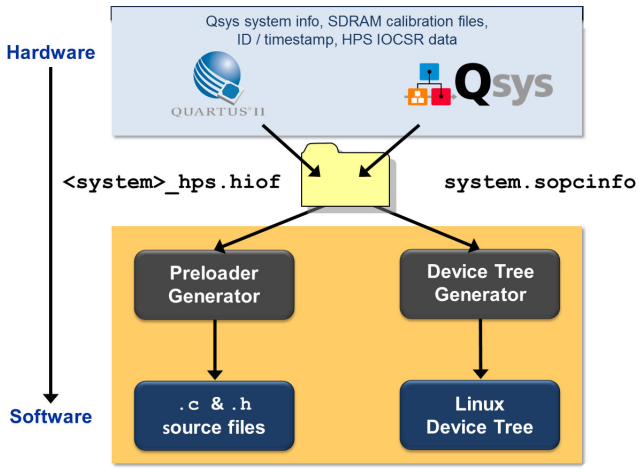
In the Altera SoC FPGAs, the FPGA looks like an FPGA, configures and works like an FPGA, and uses a standard Altera FPGA development flow including Quartus® II, Qsys, SignalTap II, System Console, and the USB Blaster. These tools will be very familiar to you if you have done Altera FPGA development before.

The ARM HPS in the Altera SoCs looks like an ARM application class processor system, works like an ARM application class processor system and uses a standard ARM development flow including GNU or ARM Cortex-A9 compiler/debugger, JTAG tools, and program trace tools. This environment will be familiar to you if you have done ARM software development in the past.



## Altera SoC Design Integration and Debugging Tools

The key advantage of the Altera SoC architecture for the hardware and software design teams is that these two analogous development flows have been coupled together by Altera, working in conjunction with ARM, to add hardware/software handoff tools as well as a FPGA adaptive debugging capability.




The hardware/software handoff tools make it easy to hand off custom hardware that is being implemented in the FPGA to the software flow so that that hardware can be integrated in to the software and generate the proper files necessary for the software to communicate with the custom hardware.

These files include the preloader files that are required by any SoC design as well as device tree files that would be needed for a Linux-based design.

For debugging this combination hardware-software system, instead of having to rely on two independent debugging tools with separate JTAG connections, the FPGA Adaptive Debugging extensions it the EDS tools allows both the ARM DS-5 debugging tool and the Altera SignalTap II tool to communicate to the SoC FPGA through a single JTAG connection provided by the Altera USB-Blaster.


This debugging architecture includes several features that are very powerful when debugging SoC designs, including:

- Single USB-Blaster target connection for software and hardware debug
- Automatic creation of register views of FPGA peripherals
- Non-intrusive trace of CPU software instructions correlated with application events and FPGA hardware events
- Hardware cross-triggering between the CPU and FPGA domains
- Simultaneous debug and trace for Cortex-A9 cores and CoreSight™ compliant cores synthesized on FPGA
- Streamline support: Statistical analysis of software load and bus traffic spanning the CPUs and FPGA

## Experience Altera SoC Advantages for Yourself

By now, it should be evident why architecture really does matter when selecting an integrated SoC design environment and that the Altera SoC architecture offers a designer many advantages in implementing an SoC design that can add value to their system.

The best way to see the advantages of the Altera SoC architecture is to implement some reference design and see for yourself how you can do designs in the FPGA logic, run simple applications in the ARM hard processor system, and implement designs that use both the HPS and FPGA logic in a combined software/hardware system.

The Mpression Helio *View* development platform available to North American customers from Macnica Americas and from other Macnica Group companies world-wide is an ideal environment for experiencing these advantages. Complete documentation is available including a "Getting Started With SoC" document that details the tools necessary and how to install them, where to get reference design files, and how to set up your Helio *View* development board. On-demand virtual workshops are also available to lead you through the design process including labs that you can implement on your desktop with your own Helio *View* board.

## Next Steps

- Learn why architecture matters in choosing an SoC FPGA platform by downloading the Altera white paper "Architecture Matters: Choosing the Right SoC FPGA for Your Application" at: http://design.altera.com/SoCweb
- Download the "Getting Started With SoC" guide for software tool and hardware board setup information from the SoC vWorkshop page: www.macnica-na.com/socworkshops or [click here to download]
- Purchase your own Helio *View* platform:
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