Getting Started with SoC

Version 2.0

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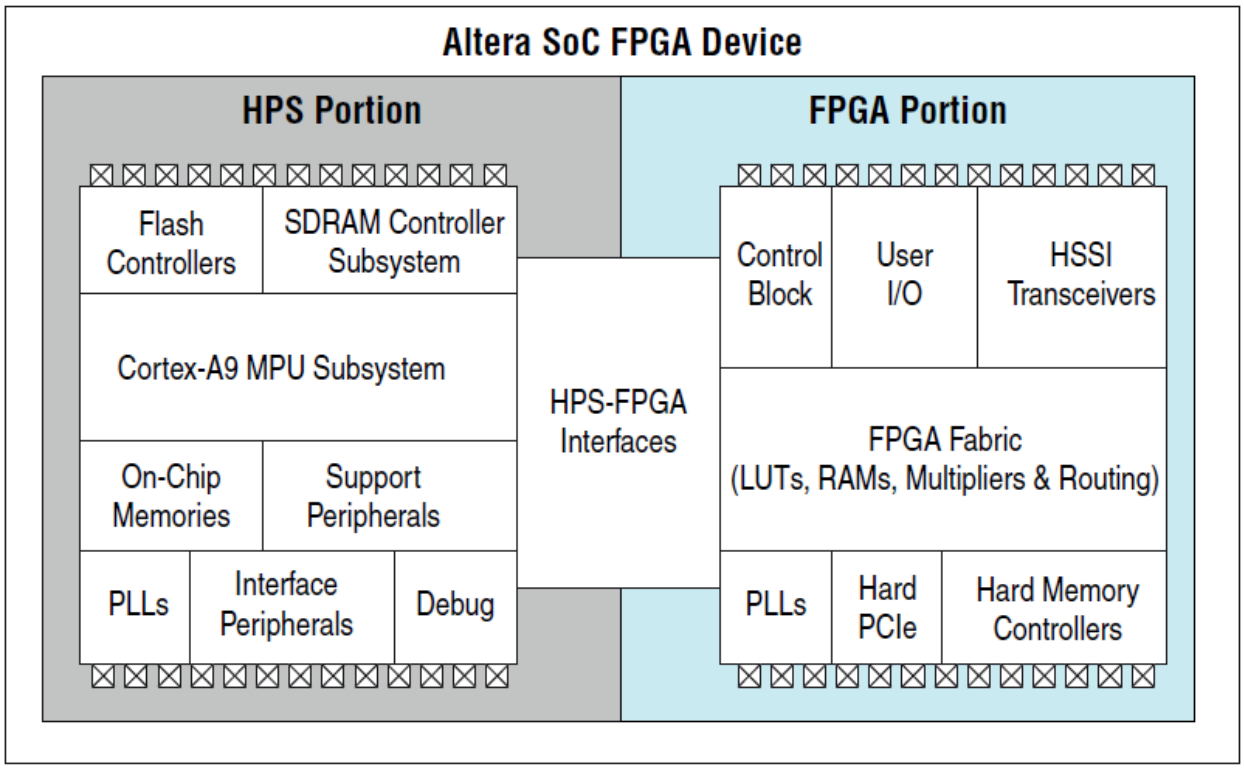
Introduction

This document is intended to help you get started using Altera's System on a Chip (SoC) device on the Mpression Helio development board. There are 5 main sections:

- SoC Overview
  - The basics of the Altera SoC devices
- Documentation
  - Where to find details on the SoC devices and development methods
- Helio Board Overview
  - A quick look at what the Helio is made up of
- Booting Linux on the Helio
  - Simple steps to get the Helio up and running a full Linux OS
- Setting up the development host
  - Details on obtaining and installing the major tools needed for SoC development

Altera SoC Overview

Altera® SoC devices integrate an ARM-based hard processor system (HPS) consisting of processor, peripherals, and memory interfaces with FPGA fabric using a high-bandwidth interconnect backbone. It combines the performance and power savings of hard intellectual property (IP) with the flexibility of programmable logic.



These user-customizable ARM-based SoCs are ideal for:

- Reducing system power, cost, and board size by integrating discrete processors and digital signal processing (DSP) functions into a single FPGA
- Improving system performance via high-bandwidth interconnect between the processor and the FPGA
- Differentiating your end product by customizing in both hardware and software
- Enhancing system reliability with built-in error correction code (ECC) and memory protection guarding your system against potential hardware or software errors
- Developing ARM-compatible software with unmatched target visibility, control, and productivity using Altera's exclusive FPGA-adaptive debugging

These devices include additional hard logic such as PCI Express, multiport memory controllers, and high-speed serial transceivers. SoCs drive down power and cost while enabling performance levels required by cost-sensitive applications.

Documentation

Altera

You can find complete documentation for the Cyclone V SoC devices here:

http://www.altera.com/literature/lit-cyclone-v.jsp

The data sheet covers the electrical specifications, switching characteristics, configuration specifications, and I/O timing for Cyclone® V devices.

Volume 1 of the handbook covers standard FPGA topics. Volume 2 covers the transceivers and volume 3 of covers the Hard Processor System (HPS).

The following interactive web-page gives the names, address and descriptions of the many (thousands) of registers in the HPS.

http://www.altera.com/literature/hb/cyclone-v/hps.html

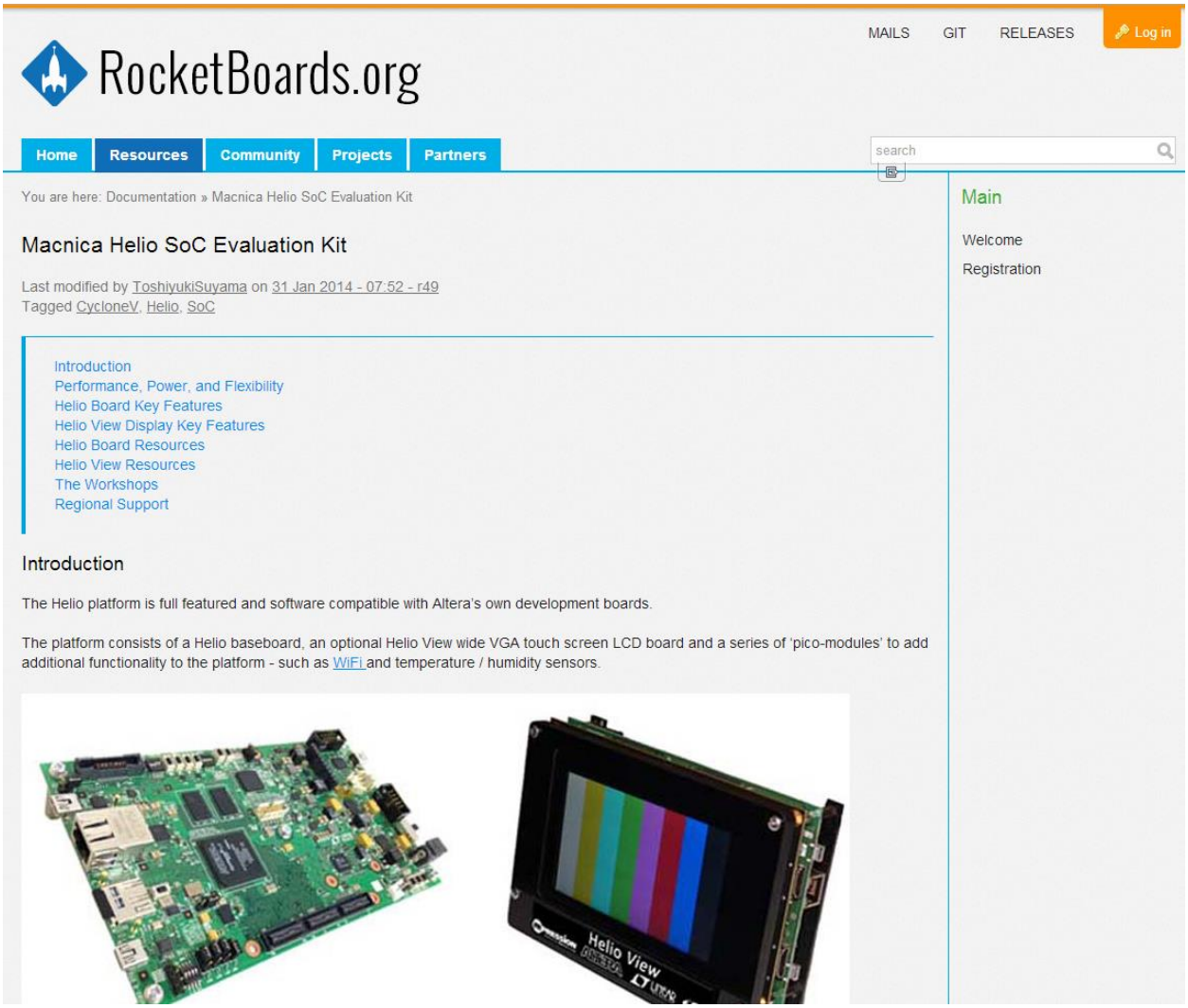
RocketBoards.org

RocketBoards.org is a SoC/Linux community supported portal. Altera and Macnica are putting anything Linux related here following the existing Linux community method of boards specific support. The portal also hosts a Wiki site, mail list server, and project repository to aggregate community resources.

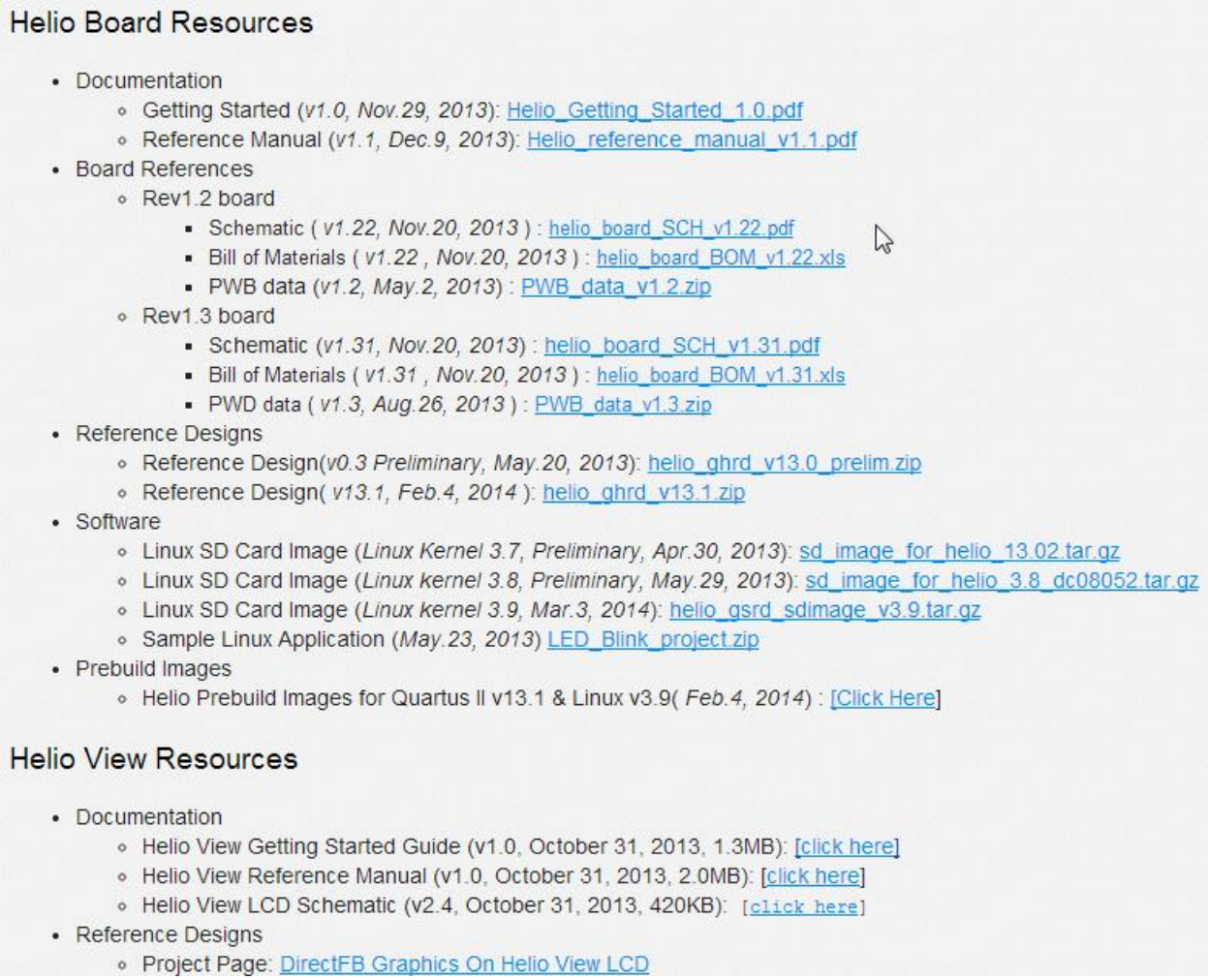
http://www.rocketboards.org/

Macnica's Helio documentation can be found on this site. The Helio board information is under "**Macnica Helio SoC Evaluation Kit**" on the main RocketBoards page.

http://www.rocketboards.org/foswiki/Documentation/MacnicaHelioSoCEvaluationKit



On the Helio page you will find a **Helio Board Resources** section as shown here:



Helio Board Resources

- Documentation
  - Getting Started (*v1.0, Nov.29, 2013*): Helio_Getting_Started_1.0.pdf
  - Reference Manual (*v1.1, Dec.9, 2013*): Helio_reference_manual_v1.1.pdf
- Board References
  - Rev1.2 board
    - Schematic (*v1.22, Nov.20, 2013*) : helio_board_SCH_v1.22.pdf
    - Bill of Materials (*v1.22 , Nov.20, 2013*) : helio_board_BOM_v1.22.xls
    - PWB data (*v1.2, May.2, 2013*) : PWB_data_v1.2.zip
  - Rev1.3 board
    - Schematic (*v1.31, Nov.20, 2013*) : helio_board_SCH_v1.31.pdf
    - Bill of Materials (*v1.31 , Nov.20, 2013*) : helio_board_BOM_v1.31.xls
    - PWD data (*v1.3, Aug.26, 2013*) : PWB_data_v1.3.zip
- Reference Designs
  - Reference Design(*v0.3 Preliminary, May.20, 2013*): helio_ghrd_v13.0_prelim.zip
  - Reference Design(*v13.1, Feb.4, 2014*): helio_ghrd_v13.1.zip
- Software
  - Linux SD Card Image (*Linux Kernel 3.7, Preliminary, Apr.30, 2013*): sd_image_for_helio_13.02.tar.gz
  - Linux SD Card Image (*Linux kernel 3.8, Preliminary, May.29, 2013*): sd_image_for_helio_3.8_dc08052.tar.gz
  - Linux SD Card Image (*Linux kernel 3.9, Mar.3, 2014*): helio_gsrd_sdimage_v3.9.tar.gz
  - Sample Linux Application (*May.23, 2013*) LED_Blink_project.zip
- Prebuild Images
  - Helio Prebuild Images for Quartus II v13.1 & Linux v3.9(*Feb.4, 2014*) : [Click Here]

Helio View Resources

- Documentation
  - Helio View Getting Started Guide (v1.0, October 31, 2013, 1.3MB): [click here]
  - Helio View Reference Manual (v1.0, October 31, 2013, 2.0MB): [click here]
  - Helio View LCD Schematic (v2.4, October 31, 2013, 420KB): [click here]
- Reference Designs
  - Project Page: DirectFB Graphics On Helio View LCD

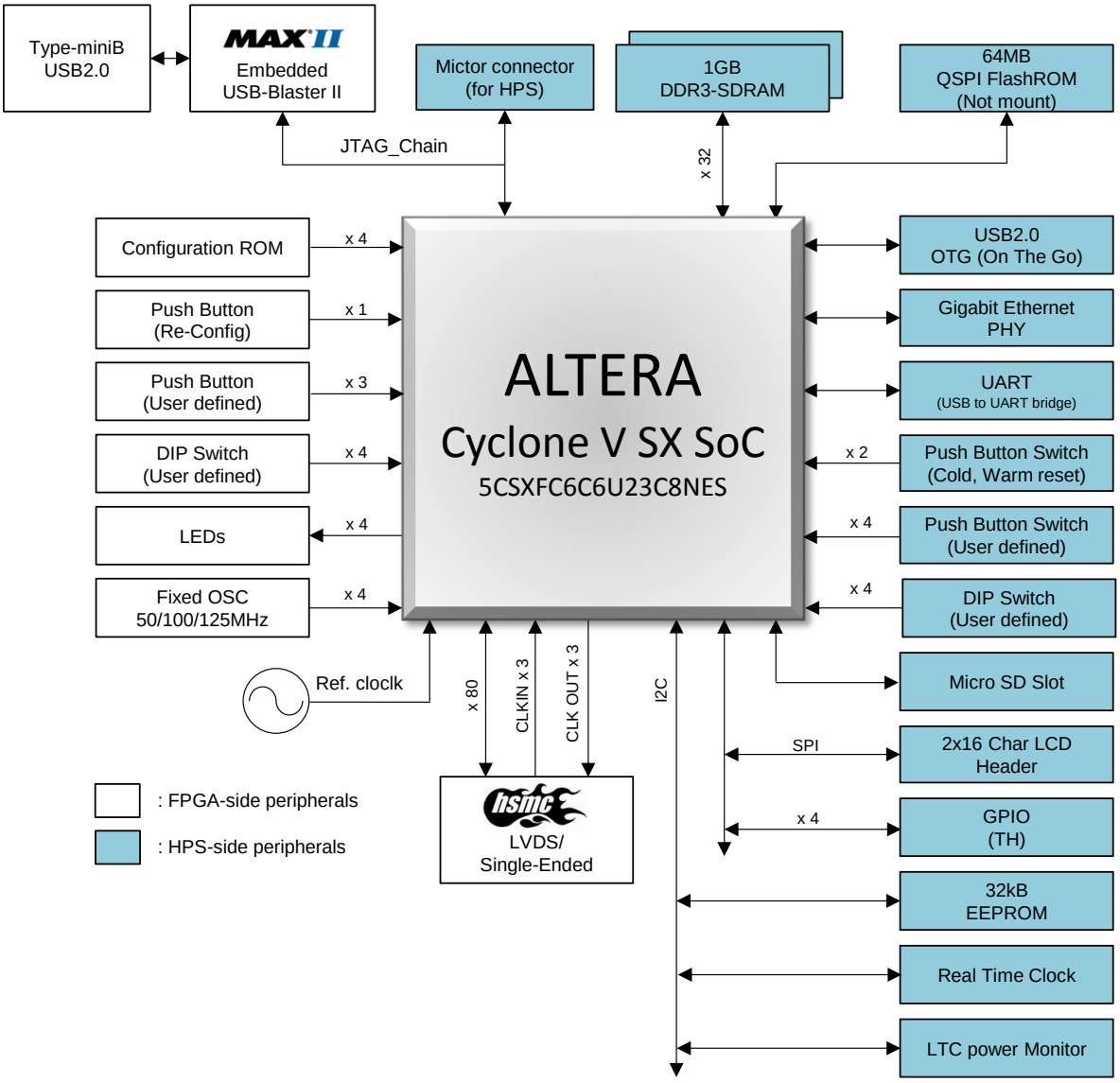
Information on the Helio board can be found in Getting_Started_Helio_1.0.pdf and Helio_reference_manual_v1.1.pdf documents. The schematics, bill of materials and board design files can be found here as well as additional reference designs and pre-build software packages.

Helio Board Overview

The Helio board is Mpression's SoC development board and the main core is the Altera Cyclone V SoC which includes the Hard Processor System (HPS) with integrated ARM Cortex™-A9 MPCore processor.

The Helio board features the following key component blocks:

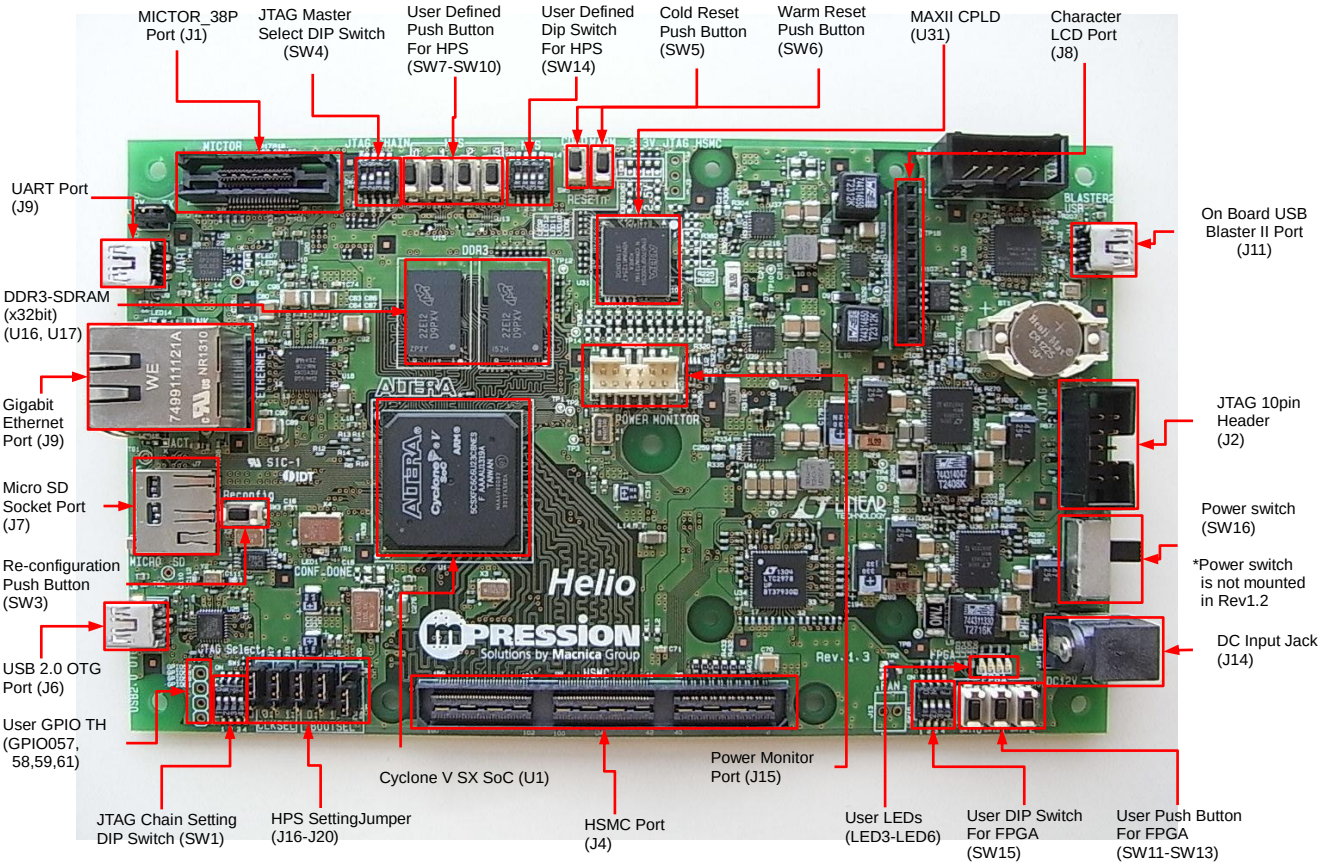
	Supplier	Function Name	Part number
CPU	Altera	SoC with FPGA	5CSXFC6C6U23C8NES
Configuration ROM	Altera	Configuration device	EPCQ256SI16N
CPLD	Altera	On-board USB-Blaster® II	EPM570GF100C5N
ROM	Microchip	EEPROM	24LC32A
RAM	Micron	DDR3-SDRAM	MT41J256M16RE
Ethernet	Micrel	Gigabit Ethernet PHY	KSZ9021RN
USB	SMSC(Microchip)	OTG USB PHY	USB3300-EZK
	Cypress	USB PHY for USB-Blaster II	CY7C68013A-56BAXC
Real Time Clock	MAXIM	I2C Real time clock	DS1339C-33#
UART	Silicon Labs	USB to UART bridge	CP2103GM
Connector	TE Connectivity	Mictor for HPS	2-5767004-2
	Samtec	HSMC	ASP-122953-01



The complete Helio Getting Started document can be found here: Helio_Getting_Started_1.0.pdf

The complete Helio Reference Manual is here: Helio_reference_manual_v1.1.pdf

Here is the top view with key features labeled:



Setting up Helio Board and Booting Linux

As shipped, the microSD card that is included with the Helio board is blank. It is possible to program the microSD card with a complete Linux image that will boot from power-on. The SoC device will be used as a standalone processor where the FPGA fabric will not be configured. The following details will be covered:

- External connections, jumper, and dip switch setting
- Load the Linux image on a microSD card
- Setup a Serial Terminal
- Watch Linux boot

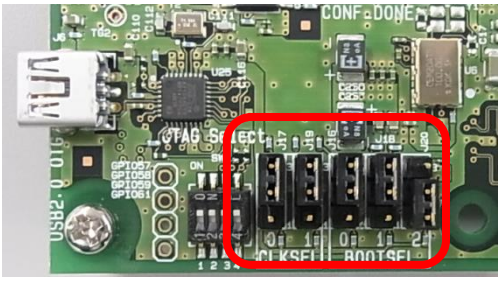
External Connections

Connect the external 12V power supply connected to J14.

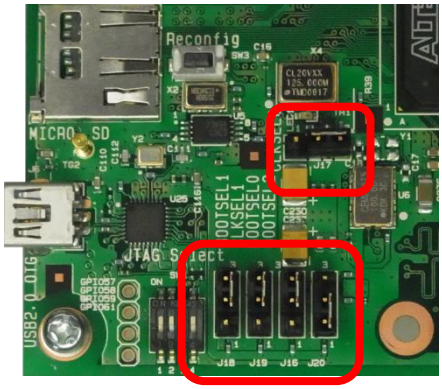
Connect a mini USB cable from host PC to J9 – USB connector (labeled UART). This is used to observe status messages from U-Boot and Linux via the serial console. Verify that J10 is OPEN.

Jumper Settings

Board Reference	Signal Name	Setting
J16	BOOTSEL0	2-3
J18	BOOTSEL1	2-3
J20	BOOTSEL2	1-2
J17	CLKSEL0	2-3
J19	CLKSEL1	2-3



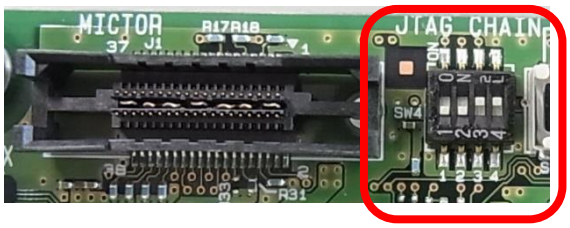
Jumper setting for Helio Rev. 1.3



Jumper setting for Heli0 Rev. 1.2

Dip Switch Settings

SW1 = all on



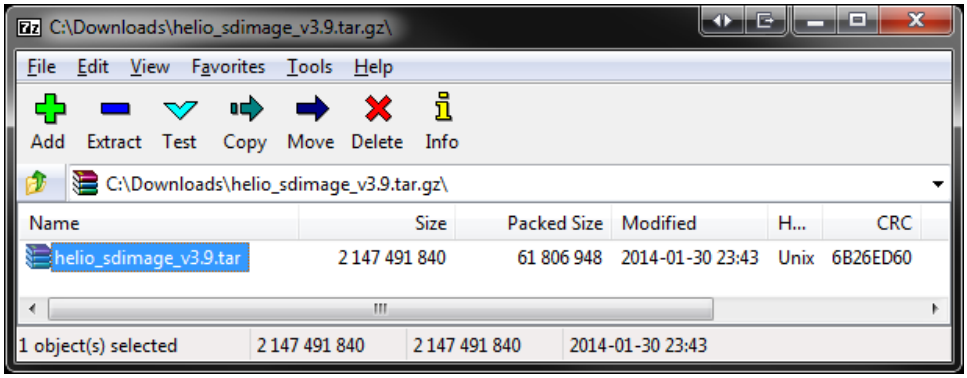
SW4 = 1-off, 2-off, 3-on, 4-on

Creating a Linux Bootable Micro SD Card

1) Download the Linux SD card image "helio_sdimage_v3.9.tar.gz". This contains a Linux image that can be copied to a microSD card. The Helio development board can boot into Linux with this microSD card. Creating this microSD card and some of the Helio board highlights will be described in the next section. helio_gsrd_sdimage_v3.9.tar.gz
2) Untar and then uncompress helio_sdimage_v3.9.tar.gz. This is a 2 step process.
    a. For Linux:

```
$ tar –xvfc  helio_sdimage_v3.9.tar.gz
```

    b. For Windows, use 7-zip or WinZip (See **Error! Reference source not found.** or **Error! ference source not found.** in the "Setting up the Host Design Environment" section of this document if you don't have one of these on your PC).



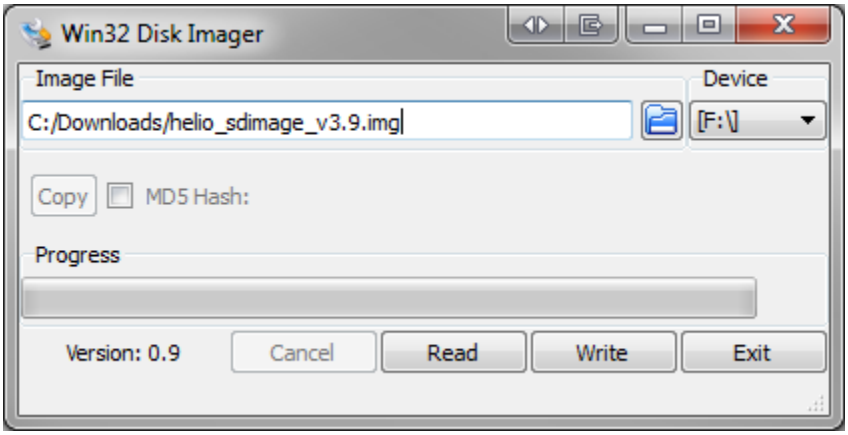
3) You will need to put the microSD card in a card reader/adapter (or USB reader). Plug the adapter into your host machine.
4) Copy helio_sdimage_v3.9.img to SD card.
    a. In Linux:

```
$ sudo dd if=sd_image_v3.9.bin of=/dev/sdx bs=512
$ sudo sync
```

Note, that the **x** is the letter of you microSD device. (Typically sda or sdb)

    b. In Windows, user Win32 Disk Imager. Click on the folder symbol to browse to the sd_image_v3.9.img file, select the device drive of your microSD card, and click "Write".

(See Win32 Disk Imager in the "Setting up the Host Design Environment" section of this document if you don't have this on your PC).



5) Once the file is copied to the microSD card, put the microSD card into the Helio microSD slot.

Serial Terminal Setup

The UART is set up as STDOUT and STDIN for the HPS. You will need a terminal program to interact with Uboot and Linux. The default SoC/Helio board UART terminal settings are:

- Baud rate: 115200
- Data bits: 8
- Stop bit: 1
- No Parity
- No Flow control

If you don't have a terminal program installed on you PC, see in the "Setting up the Host Design Environment" section of this document if you don't have this on your PC. Note that HyperTerminal is not part of Windows 7.

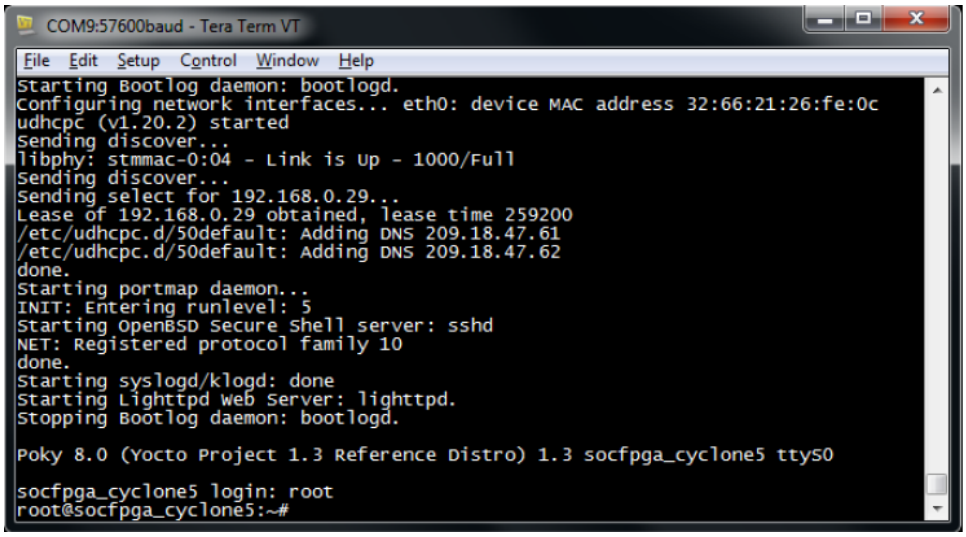
It is not necessary to load an FPGA image into the FPGA portion of the SoC in order to get Linux to boot. The two portions of the SoC device can operate completely independently until you need to open a path between them.

Running Linux

The sd_image_v3.9.img that is now programed into the microSD card is a fully functioning Linux environment encompassing the following:

- Preloader
- U-Boot Boot Loader
- Linux Kernel v3.9
- Device Tree Blob
- Root File System

1. Power-up the board using PWR switch.
2. Observe boot-up status messages in terminal window.
3. After successful boot, Linux will ask for the login name. Enter root and press Enter.



Setting up the Host Design Enviroment

The development tools that need to be installed are:

- Altera's Quartus-II FPGA Tools – Altera Complete Design Suite (ACDS)
- Altera's SoC Embedded Development Suite (SoC EDS)
- ARM's Development Studio 5 (DS-5)

The operating system you run these tools is important. Note that Altera supports Windows 7 and XP (32/64), Red Hat Enterprise 5 (32/64), and Red Hat Enterprise 6 (64) operating systems. The operating system requirements are shown at this link:

http://www.altera.com/download/os-support/oss-index.html

You will find information on how to download and install each tool in this section. Also, Windows users will want to take a look at the section on Virtual Linux Eviroment for a description of a virtual machine. It is highly recommended to develop a Linux embedded system using a Linux host. Setting up a virtual Linux machine is described in the accompanying Macnica document titled Creating_CentOS_VM.pdf.

Here is a recommend order of installation for Windows users:

1. **Error! Reference source not found.** (helps untar and unzip files)
2. Image Writer for Windows (writes Linux image/binary files to Micro SD)
3. Terminal Programs (Serial Terminal – Helio board UART interface)
4. Quartus II
5. SoC EDS/DS-5

Linux users follow this order of installation:

1. Quartus II
2. SoC EDS/DS-5
3. Setup environment variables

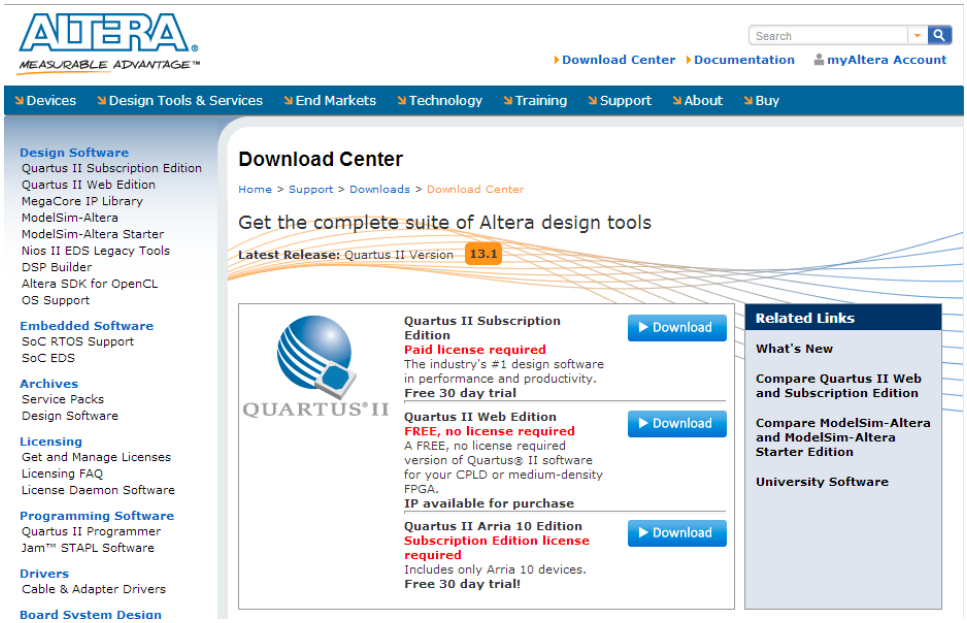
Quartus II

Quartus II is Altera's FPGA development tool. It runs on both Windows and Linux hosts. It comes in a subscription or web (free) edition. A comparison between the Subscription and Web edition of Quartus is described in this document:

http://www.altera.com/literature/po/ss_quartussevswe.pdf

The current release of Quartus II is 13.1 and it can be downloaded from this site:

https://www.altera.com/download



Refer to the Altera Quartus Installation documentation to install and license ACDS:

http://www.altera.com/literature/manual/quartus_install.pdf

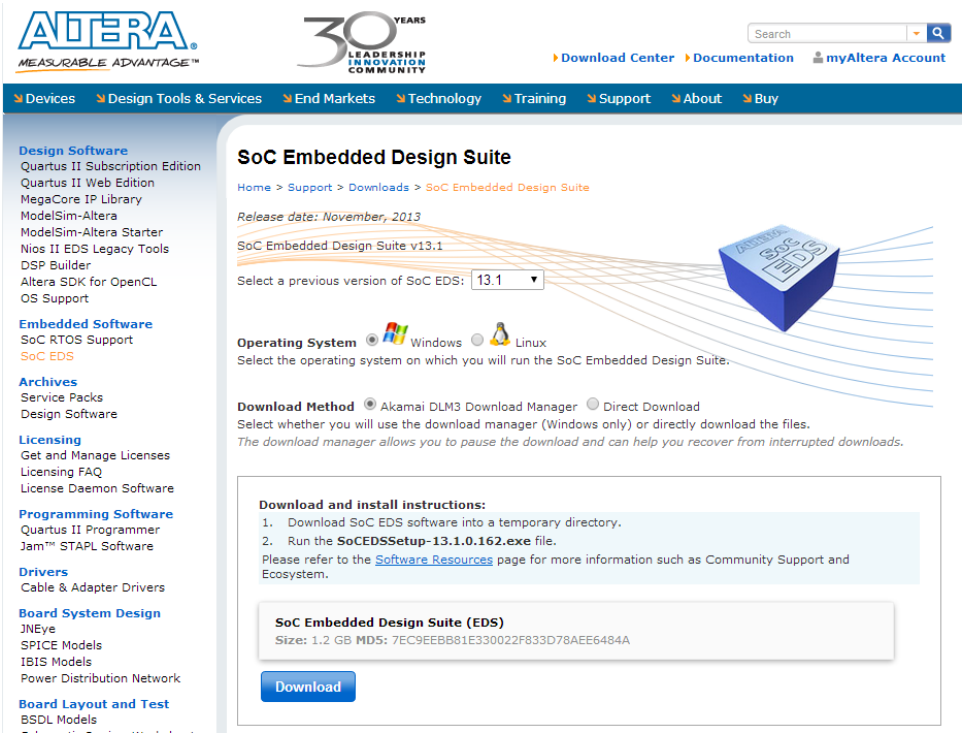
SoC EDS/ARM DS-5

The SoC EDS is a comprehensive tool suite for embedded software development on Altera SoC devices. It contains development tools, utility programs, run-time software, and application examples to expedite firmware and application software development. An Altera only version of ARM's Development Stuido 5 (DS-5) is included in the SoC EDS install. They both run on Windows and Linux hosts. It comes in a subscription or web (free) edition. A comparison between the Subscription and Web edition of SoC EDS is shown below.

Component	Key Feature	Web Edition	Subscription Edition
ARM Development Studio 5 (DS-5) Altera Edition Toolkit	Eclipse IDE	x	x
	Debugging over Ethernet (Linux)	x	x
	Debugging over USB-Blaster II (JTAG)		x
	Automatic register views		x
	Hardware cross-triggering		x
	CPU/FPGA event correlation		x
Hardware/Software Interface Tools	Preloader Support Package Generator	x	x
	Device Tree Generator*	x	x
Compiler Tools	Linaro Linux GCC tool chain (arm-linux-gnueabihf-)	x	x
	Mentory CodeBench Lite Bare-metal GCC tool chain (arm-none-eabi-)	x	x
SoC Hardware Libraries	HWLibs	x	x
SoC Programming Examples	Golden Hardware Reference Design, variety of software and Linux examples	x	x

The current release of SoC EDS is 13.1 It can be downloaded from this site:

https://www.altera.com/download/software/soc-eds



Refer to section 2 of the Soc EDS Users Guide to install SoC EDS:

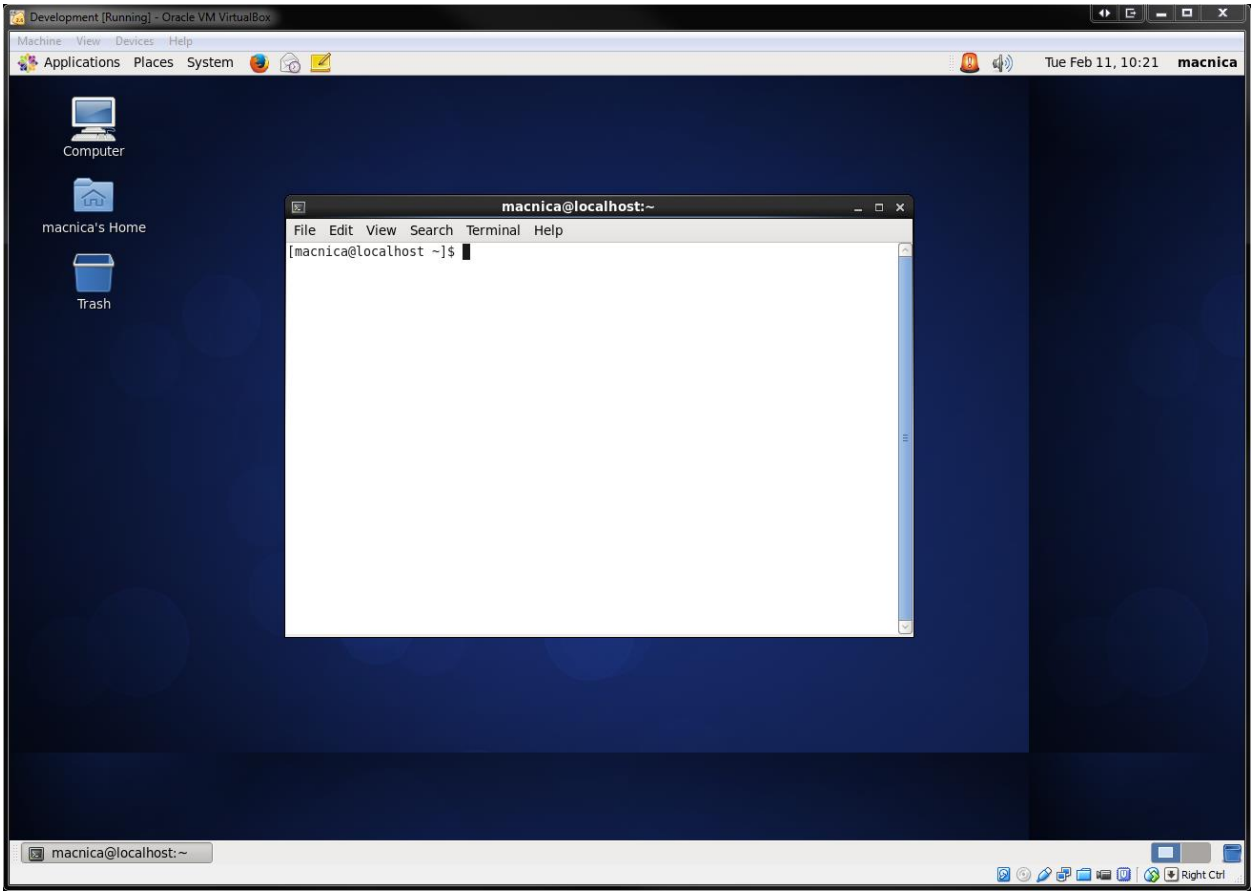
http://www.altera.com/literature/ug/ug_soc_eds.pdf

Virtual Linux Eviroment

If you use a supported Linux host, you can skip this section. If you plan to run Linux on the SoC and your host PC is Windows based, you may want to set up a virtual Linux enviroment. Some things are easily done in Linux which are more difficult in Windows. Setting up a virtual machine gives you the best of both worlds.

Macnica highly recommends using Red Hat or CentOS linux distribution to run the SoC EDS. Macnica's techincal staff is using Oracle's VirtualBox and CentOS. Both VirtualBox and CentOS Linux distributions are community supported and are freely available. www.virtualbox.org

These tools are well established. Also, the Altera SoC EDS is tested on the CentOS Linux distribution. One last important note, "a prominent North American Enterprise Linux vendor" (Red Hat) has provided the kernel source code for CentOS. Below is a screenshot of a Virtual CentOS machine running on a Windows Host. Looks and feels like a Linux machine. Well it virtually is!

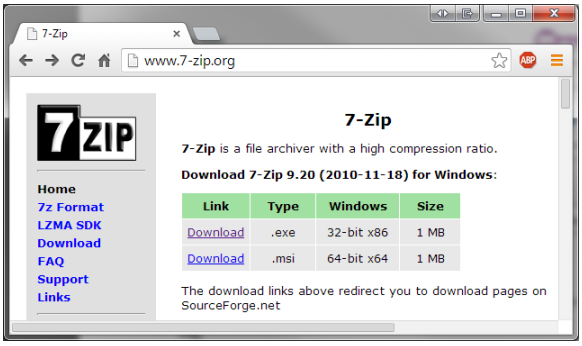


The process for setting up a CentOS virtual machine is documented in Creating_CentOS_VM.pdf

Decompression Tools

7zip and WinZip are tools that allow Windows users to unzip and untar files.

7zip is free and can be downloaded from: http://www.7-zip.org/

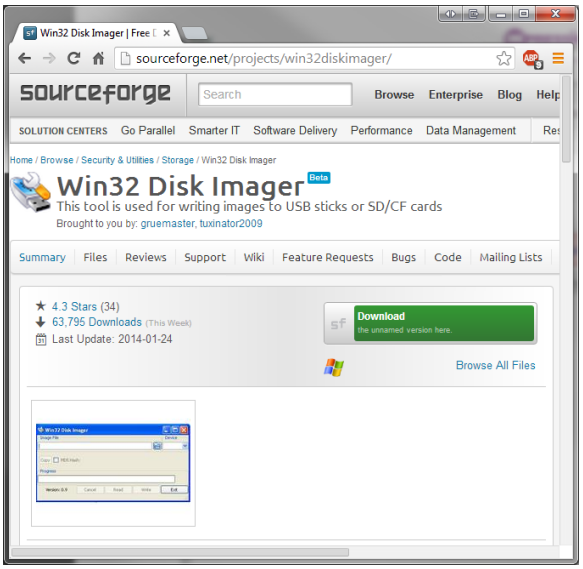


Winzip can be downloaded from: http://www.winzip.com/. It has a 30 day free trail. After the trial, it costs $29.95.

Image Writer for Windows

Win32diskimager is a free tool that allows Windows users to write binary images to SD cards. It can write full images to SD cards in just a few minutes. Windows users will need this tool to build bootable Linux microSD cards for the Helio board.

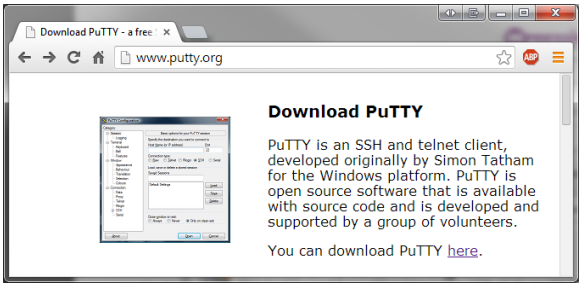
It can be downloaded from: https://launchpad.net/win32-image-writer or from http://sourceforge.net/projects/win32diskimager/



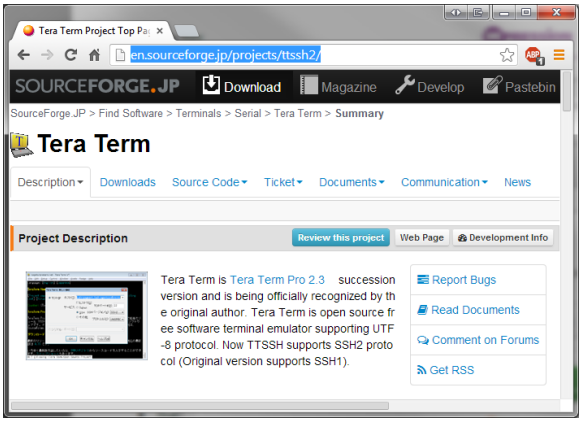
Terminal Programs

In Windows 7 and Vista, you will no longer find the HyperTerminal program. You need a serial terminal program to connect the Helio UART. There are several new alternatives to HyperTerminal. Putty comes with a serial terminal. Also, Teraterm is commonly used.

Putty can be downloaded from: http://www.putty.org/



Teraterm can be downloaded from:http://en.sourceforge.jp/projects/ttssh2/



Drivers

Install Device Driver for USB-to-Serial Chip

The Helio board has a UART to USB chip from Silicon Labs. The driver should load automatically when you connect a USB cable from your Windows machine to the Helio board. Be sure to connect the USB cable to the connection labeled UART.

If the driver does not install automatically, here are the necessary steps to install on Windows 7 machine:

1. Go to http://www.silabs.com/products/mcu/Pages/USBtoUARTBridgeVCPDrivers.aspx and download the VCP Driver Kit archive file.
2. Extract the downloaded archive and execute one of the installer files:
    a. *Run CP210xVCPInstaller_x64.exe if you have a 64 bit OS, or
    b. *Run CP210xVCPInstaller_x86.exe if you have a 32 bit OS

Install Device Driver for USB Blaster II

The Helio board includes an integrated on-board USB-Blaster II circuitry for FPGA programming and system debug. However, for the host computer and board to communicate, you must install the USB-Blaster II driver on the host computer. The drivers should be installed automatically when the ACDS is installed, but if you have issues you can manually install them as well.

Installation instructions for the USB-Blaster II driver for your operating system are available on the Altera website. Go to the Altera website: http://www.altera.com/download/drivers/dri-index.html

Table 1. Windows Driver Information for Altera Hardware (1)

Product	Windows 7/ Windows Vista (32-/64-Bit)	Windows XP (32-/64-Bit)	Windows NT	Windows 2000	Windows 98
EthernetBlaster cable *EthernetBlaster Communications Cable User Guide* (PDF)	Upgrade firmware	Upgrade firmware	Upgrade firmware	Upgrade firmware	Upgrade firmware
EthernetBlaster II cable *EthernetBlaster II Communications Cable User Guide* (PDF)	Upgrade firmware	Upgrade firmware	Not supported	Not supported	Not supported
USB-Blaster™ cable *USB-Blaster Download Cable User Guide* (PDF)	Install driver	Install driver	Not supported	Install driver	Not supported
On-Board USB-Blaster™ II cable	Install driver	Install driver (3)	Not supported	Not supported	Not supported

Table 2. Linux and UNIX Driver Information for Altera Hardware

Product	Linux (32-/64-Bit)	Solaris	HP-UX
EthernetBlaster cable *EthernetBlaster Communications Cable User Guide* (PDF)	Upgrade firmware	Upgrade firmware	Upgrade firmware
EthernetBlaster II cable *EthernetBlaster II Communications Cable User Guide* (PDF)	Upgrade firmware	Not supported	Not supported
USB-Blaster cable *USB-Blaster Download Cable User Guide* (PDF)	Set port permissions	Not supported	Not supported
On-Board USB-Blaster II cable	Set port permissions	Not supported	Not supported

Notes

Document Revision History

Revision	Date	Comments
0.1		Initial Draft
0.2		Internal Review
1.0		Customer Release
2.0	March 19, 2014	Updated to v2.0